

Appln. No.: 10/762,156  
Amend/Response After Final, filed May 14, 2007  
Replying to Office Action of Feb. 14, 2007

PATENT  
MS: AFTER FINAL  
A.U. 2811 – Expedited Processing Requested  
Attorney Docket No. 352003-991320

### REMARKS

In reply to the final Office Action of February 14, 2007, Applicants respectfully request consideration of the following remarks. Claims 1-13 are pending in this application, with claims 7 and 9-13 withdrawn.

In the Office Action, the Examiner (i) rejected claims 1-6 and 8 under 35 U.S.C. §103(a) as being unpatentable U.S. Patent No. 6,262,487 over Igarashi *et al.* ("Igarashi") in view of Applicant Admitted Prior Art (AAPA). Reconsideration is respectfully requested.

#### Rejections Under 35 U.S.C. §103(a)

Claims 1-6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Igarashi in view of AAPA.

Applicants respectfully request reconsideration of these rejections because, with regard to independent claim 1, Igarashi fails to teach or suggest a second buffering cell adjacent to "a second side adjacent to the first side of the function block" as well as "signal wiring passing over the function block obliquely relative to the first side and the second side," among other things. Similarly, with regard to independent claim 8, Igarashi also fails to teach or suggest cell arrangement and wiring limitations consistent with those of claim 1.

Specifically, the Examiner's comparison of Igarashi to the claims, as understood by Applicants, is illustrated in the drawing attached hereto at Tab A. As best understood, it appears that the Examiner is arguing, first, that cells of Igarashi corresponding to the first and second buffering cells (see 183A and 183B of Tab A) are arranged in the claimed relation to the function block (see callout 80 of Tab A), and, second that the wiring 162 of Igarashi passes over the function block, as also set forth in claim 1.

With regard to the first point, Applicants respectfully submit that Igarashi (see, i.e., Fig. 13C) does not disclose a first side of the function block being adjacent to the first buffering cell and a second side of the function block, adjacent to the first side,

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being adjacent to the second buffering cell. Instead, the arrangement of Igarashi is shown at Tab A. In the claimed invention, the first side of the function block and the second side of the function block are adjacent each other, and the first side of the function block is a side of the function block and the second side of the function block is another side of the function block. In other words, the first buffering cell is arranged at a side of the function block and the second buffering cell is arranged at another side of the function block. However, each of a plurality of buffering cells according to Igarashi Fig. 13C is arranged at the same side of the function block. Therefore, because the recited arrangements of function blocks and cells are not met, Igarashi cannot render the claimed invention obvious for this first reason.

With regard to the second point, Applicants respectfully submit that wiring 162 of Igarashi does not pass over the function block, but, rather, only over wiring 161. Here, figures 13A and 13B are helpful interpreting Fig. 13C. The sequence illustrated in Figs. 13A-13C shows the process that starts in the initial state of Fig. 13A and goes through the state shown in Fig. 13B to reach the state shown in Fig. 13C. The route of the wiring 162 is changed so that the wiring 162 includes the oblique wiring 173 and the oblique wiring 174, in Fig. 13B. This routing change is done to shorten the distance of parallel lines provided by wirings 161 and 162 arranged in the same layer. Wiring 162 achieves the routing change by passing over the wiring 161 vis-à-vis the oblique wiring 173 and the oblique wiring 174 portions. Thus, wiring 162 passes over the wiring 161 in the oblique wiring 173 portion and oblique wiring 174 portion, not the function block. Indeed, the placement/existence of the bottom cell block 80 does not even bear relation to the cited portions of Igarashi to show anything further. Therefore, because the recited arrangements of function blocks and cells are not met, Igarashi cannot render the claimed invention obvious for this second, independent and distinct reason.

With regard to the combination of the "Applicants Admitted Prior Art" (AAPA) with Igarashi in the context of the present § 103(a) rejection, the alleged AAPA fails to cure the deficiencies in Igarashi noted above. For example, AAPA is cited by the Examiner only for the sake of showing interconnection and wiring length, regarding which

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Applicants disagree, and believe to be both logically incomplete and improper. Here, *inter alia*, AAPA fails to teach or suggest the suggested claimed cell arrangement and wiring limitations.

Therefore, Applicants respectfully request that the rejections of claims 1-6 and 8 under U.S.C. § 103(a) be withdrawn and the claims allowed.

Conclusory Remarks

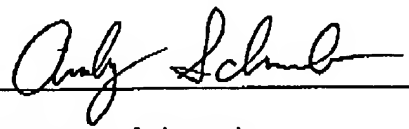
In view of the above, it is respectfully submitted that claims 1-6 and 8 are in condition for formal allowance, and early and favorable action to that effect is respectfully requested.

The Examiner is invited to call Applicants' attorney at the number below in order to expedite the prosecution of this application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. 07-1896 referencing Attorney Docket No. 352003-991320.

Respectfully submitted,  
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Dated: May 14, 2007

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Attachments: Tab A – Diagram regarding cited art

Tab A

